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A 64-Channel Neural Signal Processor/ Compressor Based on Haar Wavelet Transform

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***Abstract*— A signal processor/compressor dedicated to implantable neural recording microsystems is presented. Signal compression is performed based on Haar wavelet. It is shown in this paper that, compared to other mathematical transforms already used for this purpose, compression of neural signals using this type of wavelet transform can be of almost the same quality, while demanding less circuit complexity and smaller silicon area.**

Designed in a 0.13-µm standard CMOS process, the 64-channel 8-bit signal processor reported in this paper occupies 113µmx110µm of silicon area. It operates under a 1.8-V supply voltage at a master clock frequency of 3.2MHz.

I. Introduction

NOWADAYS, implantable neural recording micro-devices are of increasing interest in neuroscience research, curing neural disorders, and also in prosthetic applications. Being implantable, means that such systems cannot have any hardwired connection to the outside. Therefore, they receive electric power and also communicate data with the outside world through wireless connection [1-3]. Large number of recording channels (in the order of hundreds of channels) is of great importance in increasing the neural information recorded as well as in enhancing the spatial resolution of the recordings. According to the available frequency allocation regulations, the frequency bands that can be used for data communication for this purpose are not unlimited in bandwidth. As a result, to transmit the data recorded on high-density electrode arrays, one needs to somehow refine or compress the signals.

To be able to handle hundreds of neural channels, in some works, only the occurrence of spikes is reported to an external host [1]. For detailed studies, it is sometimes useful to telemeter waveshape of action potentials. The processor reported in [2] detects neural spikes based on automatic calculation of two threshold levels to compare the signal with. To be able to telemeter as much information as possible from a neural recording implant to the outside world, digital signal processing (DSP) techniques have proved to be effectively useful. From among the different possible DSP solutions, mathematical transforms such as Walsh-Hadamard transform [4] and discrete wavelet transform [5-7] have been recently employed successfully.

This work proposes discrete wavelet transform with Haar basis function for the processing and subsequently compression of neural signals. This proposition is mainly because of simpler and more compact electronic implementation compared to other techniques, which leads to smaller physical size and lower power consumption.

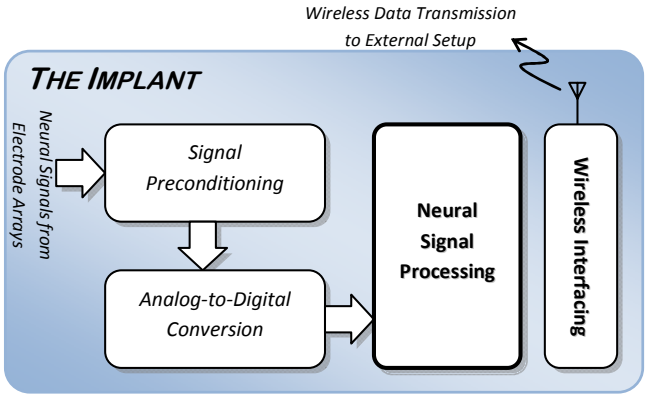

Fig. 1: Signal processor in an implantable neural recording device

II. System Description

Fig. 1 shows a simplified general block diagram for a typical implantable multi-channel neural recording micro-device. After signal preconditioning and conversion from analog form into digital domain, multiple neural signals are then delivered to a neural processor. Such a processor usually performs data reduction/compression techniques and algorithms in order to more efficiently utilize the limited bandwidth available for wireless data telemetry to the outside world.

The digital neural processor presented in this paper is designed for a 64-channel neural recording system. The neural signals sensed by an electrode array are amplified with a gain of ~60dB, band-pass filtered with a pass band of around 10Hz to10kHz, and digitized with a resolution of 8

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bits at 20kSample/Sec. The processor is designed to reduce the amount of telemetered data by preserving action potentials and discarding the background noise.

III. Data Compression Technique

Discrete wavelet transform (DWT) has been already introduced as a successful approach for the compression of neural signals. For instance, DWT with symmlet4 basis function is reported in [5,6] as a successful data compression algorithm in neural recording. It is believed that symmlet4 was preferred to other basis functions in this specific application because of its similarity to the wave shape of action potentials in neural signals. Price of the exceptional data compression using this basis function is, however, paid by rather considerable circuit complexity. This is translated into large silicon area and high power consumption when the circuit is physically implemented. These drawbacks are not welcomed in implantable neural recording microsystems, where small physical size and low power operation are of crucial importance. The digital multipliers required to realize DWT with basis functions such as high-order *Daubechies* and *symmlet* are indeed the main cause of the problem. Although smart circuit solutions have been proposed in [5] to overcome this issue, signal processing circuitry for neural recording implants yet need to be more compact in size and less power consuming, especially for high density recording (i.e., large number of neural channels).

In this paper, discrete *Haar* wavelet transform (DHWT) is proposed for neural signal processing. Haar basis function may not perform as efficient in data compression as complex functions such as some of high-order *Daubechies* and *symmlet*, but it is implemented with much less circuit complexity. This is of crucial importance in the design of implantable devices.

In the case of a two-point DHWT, for every two consecutive signal samples, *S(2m)* and *S(2m+1),* two coefficients are defined as:

$$C_A(m) = \frac{1}{\sqrt{2}}[S(2m) + S(2m+1)] \quad (1.a)$$

and

$$C_D(m) = \frac{1}{\sqrt{2}}[S(2m) - S(2m+1)] \quad (1.b)$$

known as *approximation* and *detail* coefficients [8]. To have a simple digital implementation, coefficients C_A and C_D are scaled by a factor of $\sqrt{2}$. As a result, calculation of DHWT coefficients reduces to simple addition and subtraction operations. Employing two-point DHWT for the compression of neural signals in a multi-channel system, DHWT coefficients for the i^{th} channel are calculated as:

$$C_{A,i}(m) = S_i(2m) + S_i(2m+1) \quad (2.a)$$

and

$$C_{D,i}(m) = S_i(2m) - S_i(2m+1) \quad (2.b)$$

Fig. 2 shows a neural signal and the associated DHWT coefficients.

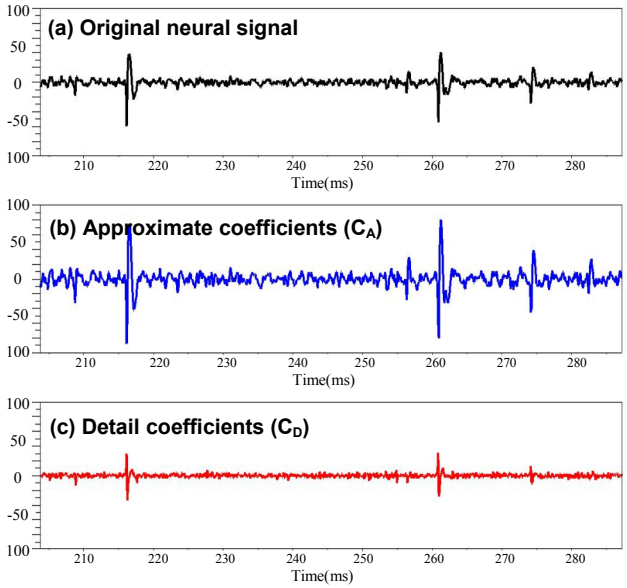

Fig. 2: Applying DHWT on a neural signal

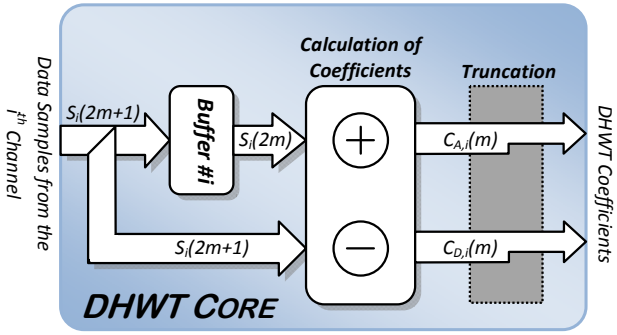

Fig. 3: Hardware implementation of the proposed DHWT core for one channel

According to equations (2.a&b), assuming that neural signals are digitized to *N* bits, DHWT coefficients will be (*N*+1)-bit digital words. As a result, DHWT itself does not reduce the amount of data. In order to reduce the amount of data being telemetered to the outside, the coefficients are truncated from the least significant side. On one hand, this introduces some error added to the signal being processed, and on the other hand, both circuit complexity and the amount of data being telemetered will be considerably reduced. It will be shown later that the gain in circuit complexity and bit rate is much more significant that the penalty paid by the noise added to the signal.

IV. Hardware Implementation

Block representation for hardware implementation of the proposed DHWT-based approach is shown in Fig. 3, according to which calculation of coefficients for two-point Haar wavelet requires only a buffer, an adder, and a subtractor.

To compare DWT in the case of Haar and symmlet4 basis functions, they are both designed in this work to process neural signals with 8 bits of resolution. Fig. 4 shows the

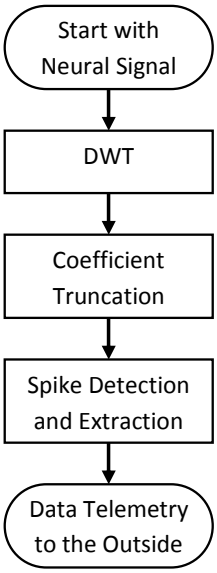

Fig. 4: Flowchart of the DWT processing performed to neural signal compression/reduction

flowchart of the signal processing plan for both cases. Neural signal is first processed using the associated basis function. As a result, in the symmlet4 case, four pairs of coefficients (approximate and detail coefficients) are generated for every eight signal samples. For the proposed Haar wavelet case, one pair of coefficients is generated for every two signal samples. In both cases, only the 5 most significant bits (MSB) of C_A and only 4 useful bits of C_D are taken to the *coefficient truncation* step. This step results in a compression rate (CR) of:

$$CR = \frac{2 \times 8}{5 + 4} = 1.78$$

As the final step to further reduce the amount of data bits telemetered off the system, only the coefficients calculated within the time intervals where spikes occur are sent to the outside.

V. Simulation and Experimental Results

To evaluate the performance of the proposed compression approach, *normalized sample-by-sample error (NSE)* is used as a measure to quantify how much the neural signal is subjected to error (mainly due to coefficient truncation) when it goes through the process shown in Fig. 4. NSE is indeed a measure to determine how well wave shape of spikes is preserved. It is defined for the time window where spikes occur as:

$$NSE_{RMS} = \frac{Error_{RMS}}{Signal_{p-p}}$$

where $Error_{RMS}$ is the error added to a certain signal sample when passing through the compression process, and $Signal_{p-p}$ is the peak-to-peak amplitude of the spike.

Table I compares the two transforms in terms of the error introduced by the transforms, compression rates, and hardware implementation details. To have a fair comparison, the same neural signal has been applied as the input to both designs. As expected, in the "Without Spike Detection" case, relative error (Error%) for DHWT is slightly larger than that for the Symmlet4 case (by 0.1%). This is mainly because Symmlet4 is a more suitable basis function for data compression as compared with the simple Haar function. The excessive error, however, is so small that can be easily neglected. Hardware implementation of the DHWT design, on the other hand, shows significant saving in the number of transistors (by 83%) and in the occupied silicon area when physically laid out in a 0.13-µm standard CMOS process (by more than 90%). It should be noted that, in Table 1, details of hardware implementation for the Symmlet4 case are presented from [5]. In the "With Spike Detection" case with almost the same compression rate, relative error for the proposed DWHT-based approach is expectedly larger than the Symmlet4 case. Again, compared to the Symmlet4-based technique, the proposed method exhibits almost the same compression rate, slightly larger (but acceptable error), and much more compact hardware implementation.

A 64-channel neural processor/compressor was designed based on the data compression approach presented in this paper. A preliminary prototype was then implemented and tested on an FPGA-based development board. To test the processor, prerecorded guinea pig neural signals sampled at

TABLE I
SINGLE-CHANNEL DWT COMPRESSION

	Without Spike Detection		With Spike Detection		Hardware (Without Spike Detection)	
	Error %	CR	Error %	CR	Area (mm^2)	No. of Transistors
Haar	1.57	1.78	2.22	112	0.0037	1348
Symmlet4	1.47	1.78	1.59	108	0.040*	7931*

* From [5]

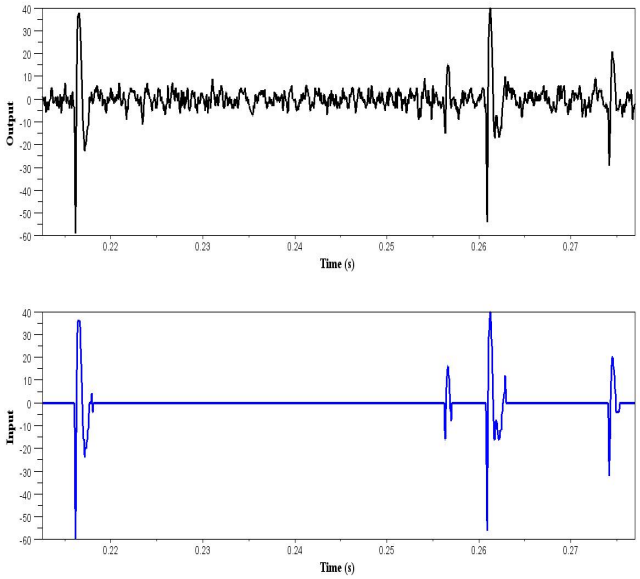

Fig. 5. Neural signal (a) before and (b) after the proposed signal processing

TABLE II
SUMMARY OF SPECIFICATIONS AND COMPARISON

	[4]	[5,6]	This Work
Transform	WHT	Symmlet4	Haar
No. of Channels	64	32	64
Signal Resolution (bits)	8	10	8
Tr. Count	N/A	42k*	16.76k
Technology	0.13µm	0.5µm	0.13µm
Area	0.185mm^2	5.75mm^2*	113µmx110µm
Compression Rate	72	62	112
Error	5%	N/A	2.22%

* Only for a 32-ch. DWT core

20kSample/Sec and digitized with resolution of 8 bits were used as input. Fig. 5 exhibits the operation of the designed DWHT-based processor in which, the top trace is the input neural signal and the bottom trace shows the signal reconstructed using the data sent off the processor (after passing through the entire process of Fig. 4).

Table II presents overall specifications of this work along with two other related works with different transforms.

VI. CONCLUSION

This paper investigates the use of discrete wavelet transform with Haar basis function for the compression of neural signals. Hardware details for electronic implementation of the proposed approach are discussed according to which, it is shown that DWHT can perform with almost the same signal processing performance as Symmlet4, while it is implemented with much simpler and more compact digital hardware.

VII. ACKNOWLEDGEMENT

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