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A Mixed Signal ECG Processing Platform with an Adaptive Sampling ADC for Portable Monitoring Applications

Hyejung Kim, Chris Van Hoof, and Refet Firat Yazicioglu

Abstract— **This paper describes a mixed-signal ECG processing platform with an 12-bit ADC architecture that can adapt its sampling rate according to the input signals rate of change. This enables the sampling of ECG signals with significantly reduced data rate without loss of information. The presented adaptive sampling scheme reduces the ADC power consumption, enables the processing of ECG signals with lower power consumption, and reduces the power consumption of the radio while streaming the ECG signals. The test results show that running a CWT-based R peak detection algorithm using the adaptively sampled ECG signals consumes only 45.6μW and it leads to 36% less overall system power consumption.**

I. Introduction

THE monitoring of biopotential signals, such as Electrocardiogram (ECG), is a common procedure in modern clinical practice. The growing interest towards the improvement of patients' quality of life and the use of biopotential signals in lifestyle applications requires the implementation of miniaturized, smart, and wireless biopotential acquisition systems with ultra-low power consumption. More advanced requirements such as more complex medical diagnostics and high accuracy analysis under ambulatory conditions drives the multi-channel sensor system design. This interest has dramatically changed how the systems for the extraction of biopotential signals are developed, putting stringent constraints on their power consumption. On the other hand, the requirement for the continuous monitoring of the patients leads to large amounts of data that needs to be processed by the DSP and/or transmitted over the radio resulting in significant power consumption. Therefore, the data compression is gaining more attention for reducing the amount of processing and the data transmitted over the radio. In this paper, we obtained data compression in ADC level. An ADC architecture with adaptive sampling and an ECG signal processing algorithm optimized to adaptively sampled input are designed to perform the required signal compression and reduce the system power consumption with very small overhead.

II. System Overview

Figure 1(a) shows the typical architecture of a smart sensor node that can be used for the signal acquisition, processing, and transmission of biopotential signals. In general, wireless sensor nodes follow two approaches for the continuous monitoring of biopotential signals:

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All authors are with imec, Kapeldreef 75, 3000 Leuven, Belgium. (corresponding author: Hyejung Kim, phone: +32-16-28-7877; fax: +32-16-28-8500; e-mail: hyejung@imec.be).

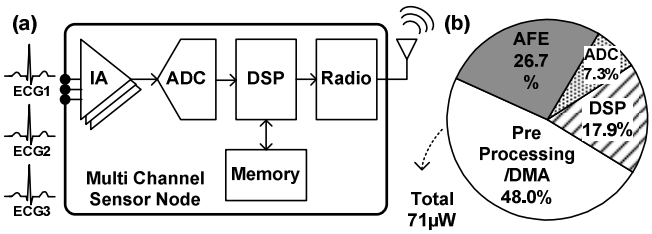

Figure 1. (a) Architecture of a multi-channel smart sensor node for biomedical signal monitoring (b) Power consumption of a mixed signal ECG processing platform when R peak detection algorithm is running

1) Data collection mode: This mode records the signals continuously and simultaneously from the selected channel, and the processing takes place at the receiver side.

2) Local processing mode: In this mode, collected signals are processed in the sensor node, i.e. additional signal filtering, ECG feature extraction, analysis, and motion artifact removal, and only result is transmitted.

The first mode suffers from the significant power consumption in the radio, where as the second mode suffers in the processing. In general, since the most power consuming part is the radio, the second approach, which is the data processing as much as possible before transmission, is more efficient method to reduce the total system power consumption.

In our previous work [1], a mixed signal ECG processing platform is designed to meet the target of configurable functionality and low power consumption. The ECG platform consists of a 5-channel (3 ECG, impedance, and band power) analog front-end (AFE), a 12-bit SAR ADC, and the custom DSP back-end using 4-way SIMD processor architecture. The ECG processing platform has been fabricated in a standard 0.18μm CMOS process and operates from a 1.2V supply. Figure 1(b) shows the power consumption when R peak detection algorithm is performed with sampling rate of 512 S/s, and the total power consumption is 71-μW. According to the pie chart in Figure 1, the power consumption for processing and memory accessing is still dominated. Therefore, more data compression should be achieved prior to the data processing stage.

This architecture presents several opportunities for the data compression. For instance, [2] has tried to implement signal compression in the analog domain, which can be the most advantageous in terms of power reduction, since it minimizes the data rate early in the signal chain. However, it relies on reducing the information content of the signal. An alternative approach is to integrate the signal compression in the ADC domain as proposed by [3, 4], leading to an output signal that requires a special DSP architecture [5] or challenging to reconstruct, respectively. In another approach,

signal compression can be accomplished in the digital domain prior to wireless transmission. Among these conventional approaches, the implementation of signal compression at the ADC level is the most attractive in terms of the trade-off between power consumption and reducing the information content of the signal.

In this work, an ADC architecture to realize an adaptive sampling, that can be used with standard DSP platforms, is designed. Furthermore, ECG signal processing algorithm optimized to adaptively sampled input is also developed to perform the required signal compression.

III. Adaptive Sampling ADC Architecture

The sampling rate of ECG signals is conventionally selected according to the high frequency region, i.e. the QRS complex. However, such constraint sampling rate over the entire ECG signal significantly increases the processing load of systems. As a solution, significant data compression without loss of information can be achieved if the sampling frequency of the ECG signals can be adapted according to the activity of the signal. For instance, QRS complex is sampled with high sampling frequency (f_H), the other region is sampled with low frequency (f_L), as shown in Figure 2.

A. *Overall Architecture*

Figure 3 shows the architecture of the adaptive sampling ADC, which consists of the two major blocks of a 12-bit ADC and an activity detector (ACTDET) block. The adaptive sampling ADC uses a standard successive approximation (SAR) ADC as a core convertor. The ACTDET consists of a differentiator, a comparator, and a multiplexer. ACTDET senses the activity of the input signal and selects the sampling rate of the ADC accordingly. In order to do that the input signal is first differentiated by using a switched capacitor (SC) differentiator. The output is digitized by a 1-bit flash ADC, passed through a digital filter, and used to select the sampling rate of the SAR ADC. For simplicity of implementation, only two frequency levels, f_L and f_H, are selected, which are respectively 64 Hz and 512 Hz for this design.

The ACTDET uses a differentiator at the front-end to extract the input signals rate of change. This choice of detecting the frequency using a differentiator stems from the fact that the use of filters to sense the activity of the input

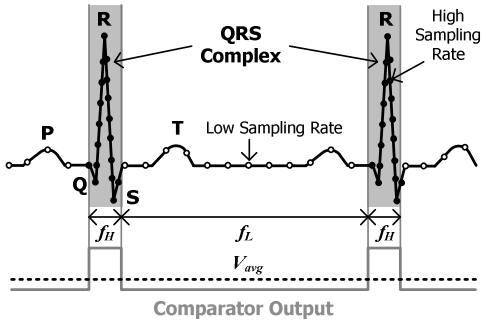

Figure 2. Principle of adaptive sampling

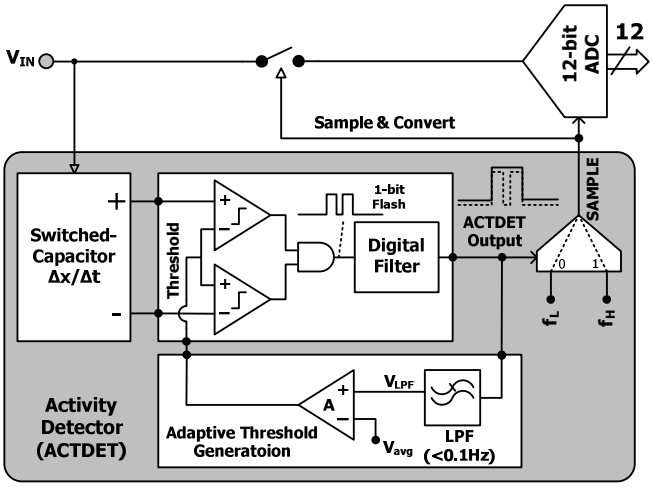

Figure 3. Proposed architecture of an adaptive sampling ADC

signal leads to significant group delay at the output of the filter according to $\tau=\omega_0/(\omega_0^2 + \omega^2)$, where ω_0 is the -3dB angular frequency of a filter and ω is the angular frequency of the input signal. This, in turn, leads to a delay in the selection of the sampling frequency. On the other hand, the group delay of an ideal differentiator is zero. Hence, the implemented ACTDET block uses a SC differentiator architecture, which is similar to the architecture in [6]. The clock frequency of the SC differentiator is 250Hz. In order to increase the update rate of the output, the actual implementation uses two differentiators operating at complementary clock phases.

B. *Adaptive Threshold Calculation*

The threshold voltage of the 1-bit flash needs to be adapted in order to detect the high and low activity regions under changing input voltage amplitudes. For ECG applications, the high frequency regions can be considered as the QRS complex of the ECG signal (Figure 2). Therefore, in an ideal operation, it is required that the ACTDET output selects the high sampling rate (f_H) during the presence of the QRS complex. The average of the ideal ACTDET output pulse can be represented by V_{AVG} and this average can be calculated since the width of the QRS complex is known. It should be noted that V_{AVG} actually corresponds to the duty cycle of the QRS complex in the complete ECG signal.

Therefore, the threshold voltage of the ACTDET can be calculated forcing the duty cycle of the actual ACTDET output to match with the calculated V_{AVG}. The negative feedback loop from the output of the ACTDET to the input of the 1-bit Flash, first computes the average of the ACTDET output block using a low-pass filter (LPF) and then compares this average, V_{LPF}, to V_{AVG}, so that the threshold voltage can be regulated to match V_{LPF} to V_{AVG}. The transfer function from the input of the SC differentiator to the output of the LPF can be written as:

$$V_{LPF}(s) = \frac{s_p}{s + (1+A)s_p}\left[V_{IN}(s)H(s) + A \times V_{AVG}\right],$$

where H(s) is the transfer function of the SC differentiator and *A* is the gain of the feedback amplifier. The LPF has been realized by an RC filter, where the R is implemented using a pseudo resistor [7]. This enables the implementation of a LPF with very low cut-off frequency, or in other words enables the average of the ACTDET output to be taken over a long period. On the other hand, the use of a large loop gain sets V_{LPF} to V_{AVG}.

IV. Measurement Results of ADC

In order to test the operation of the adaptive sampling ADC, the synthetic signal the real ECG signals are fed to the input of the ADC and the duty cycle of the comparator output pulse is monitored. Figure 4 shows the linear relation between the duty cycle of the comparator output pulse and the input V_{AVG}. And compression ratio (CR) is also shown, while changing the V_{AVG} input of the ACTDET block from 500mV down to 50mV. The duty cycle of high sampling rate range is 10% and the compression ratio is increased up to 4.5:1, when V_{AVG} is selected as 50mV causing the ADC to increase the sampling rate from 64Hz to 512Hz only during the presence of the QRS complex.

Figure 5 shows the operation of the ADC in a real monitoring application, when V_{AVG} is set to 10% duty cycle for the ACTDET output pulse. The ADC increases its sampling rate during the QRS complex and the high activity regions (motion artifact signals). Thanks to the averaging over a long period, the presence of motion artifacts does not affect the sampling of the QRS complex with high sampling rate. This sampling scheme leads to a 3 times improvement on the average data rate, which can significantly reduce power consumption for further stage of both the processing and the wireless transmission.

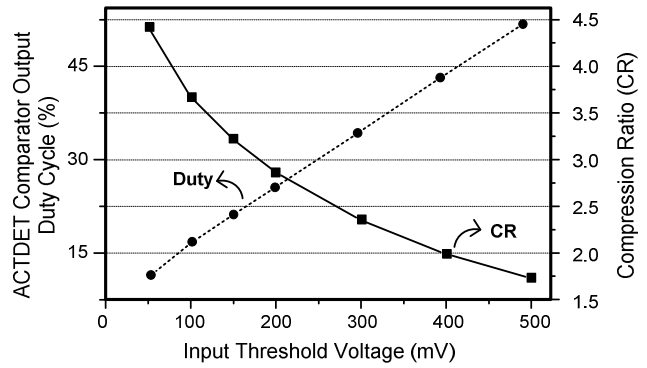

Figure 4. The control of the activity detectors duty cycle and compression ratio (CR) with changing threshold voltage (V_{AVG})

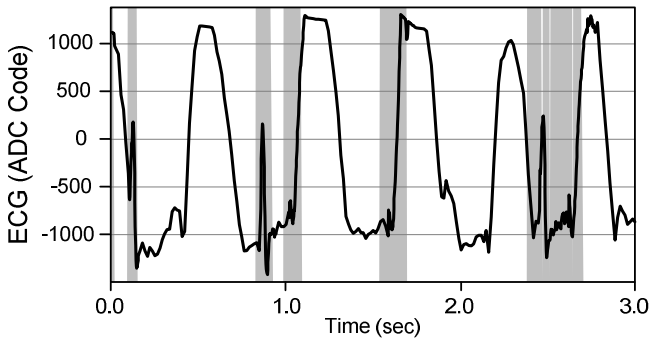

Figure 5. Measured waveform of adaptively sampled signal. Grey regions shows 512Hz sampling rate, everywhere else is sampled with 64Hz.

V. Processing Adatively Sampled Signals

A. *CWT-based R Peak Detection Algorithm*

The key benefit of such an adaptive sampling scheme is its effect on the average data rate that the system needs to process and/or transmit over the radio. In order to quantify the benefits of our approach, the continuous wavelet transform (CWT) based R peak detection algorithm [8] has been optimized adaptively sampled input signal and has been integrated into mixed signal ECG processing platform.

Figure 6 shows the functions along with its simplified block diagram. The adaptively sampled ECG signal (f_L=64Hz and f_H=512Hz) is time-stamped and streamed to the DSP for further processing. To achieve high accuracy, the motion artifacts removal algorithm is implemented before the feature extraction stage to enhance the signal reliability and analysis performance. In this work, adaptive filtering using 4th order LMS filtering is applied for motion artifact removal. The skin impedance signal, which has a high correlation to the motion artifacts [5], is monitored simultaneously with ECG signal and fed to LMS filter as a noise reference signal.

A CWT algorithm with Mexican-hat wavelet function [8] is employed to detect the R peak point for more complex medical diagnostics like heart-rate variability (HRV) analysis. However, it leads to large power consumption in the DSP due to the complexity of the algorithm and the high data rate. The ECG signal, adaptively sampled by the presented ADC, is fed to the algorithm tailored to process adaptively sampled ECG signals. The only modification has been done to the front-end of the algorithm, i.e. the convolution of the ECG signal with the mother wavelet. Since the convolution algorithm the most time consuming function and has quadratic computational complexity, $O(n^2)$, so as explained in Figure 7, adaptive sampling significantly reduces the number of multiplications and the memory access during the convolution.

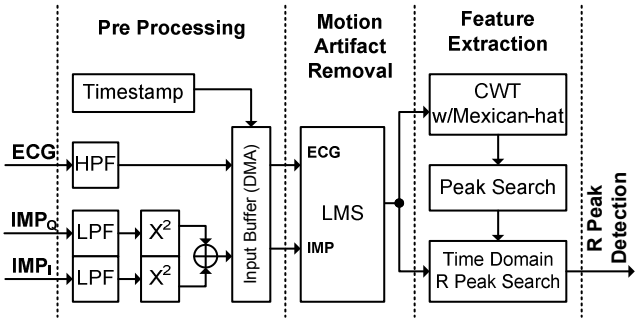

Figure 6. Flow graph of the ECG signal processing algorithm for accurate R peak detection using motion artifact removal

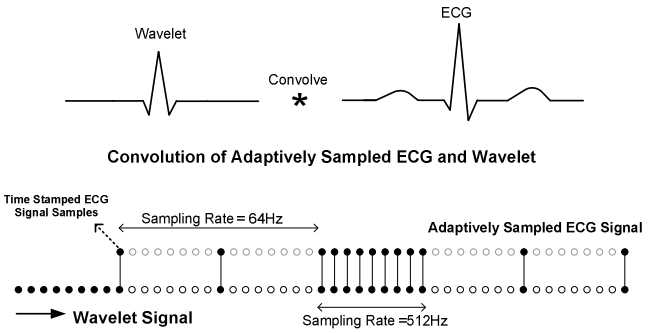

Figure 7. Applying CWT to an adaptively sampled ECG signals

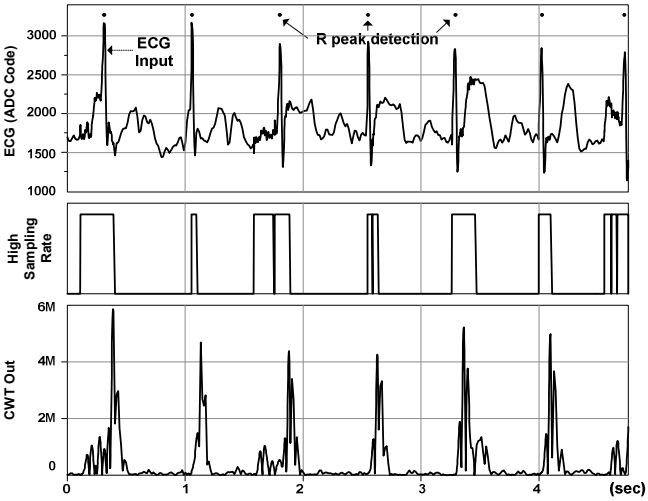

Figure 8. Measured waveform of R Peak detection processing with adaptively sampled ECG signal

The peak of CWT output gives information of presence of a QRS complex in time domain. Afterward, the exact R peak is found using a time domain peak search. The results are reconstructed with timing information of samples. Figure 8 shows the measured waveforms when a proposed CWT-based R peak algorithm with adaptively sampled signal is applied. We can see that accurate the performance of R peak detection is achieved without any performance degradation.

B. *Performance Evaluation Results*

Figure 9 shows effectiveness of the proposed adaptive sampling scheme on the mixed signal ECG processing platform. The overall operating cycle without adaptive sampling is 53k cycle/sec. It is reduced by 18k cycle/sec with adaptive sampling, which saves factor of 3 times. The number of memory access including program memory and data memory is reduced 3.2 times as well. The power consumption of the processing using adaptive sampling equivalent to 15% data rate of the full sampling rate corresponds to 50% power reduction in the DSP domain. The overall system power is reduced by 45.6 μW reduced it leads to 36% less overall system power consumption with the adaptive sampling.

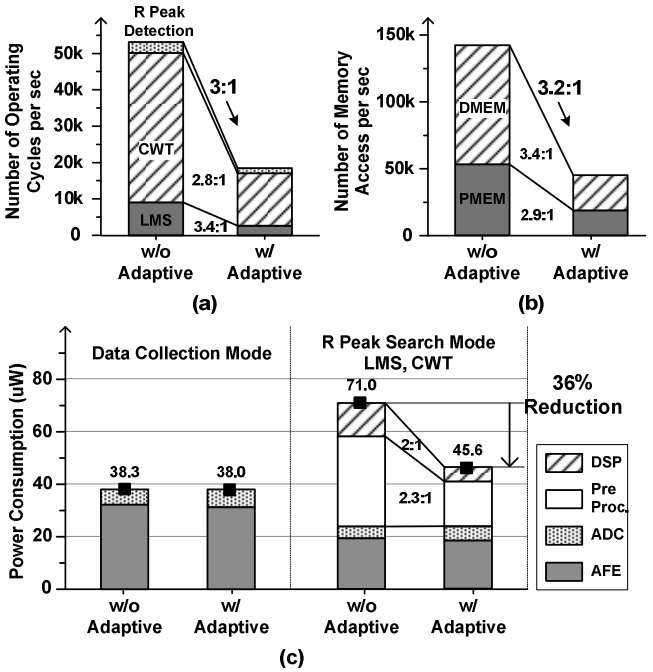

Figure 9. Performance comparison with presented adaptive sampling scheme (a) number of operating cycle (b) number of memory access (c) power consumption

VI. CONCLUSIONS

This paper presents an adaptive sampling ADC convertor architecture. This smart ADC architecture is capable of changing the sampling rate of the input signal according to the rate of the change of the signal. Such an adaptive sampling approach significantly reduces the equivalent data-rate of the ADC output without affecting the information content of the input signal. The CWT-based R peak detection algorithm has been demonstrated by to be a reliable approach for the processing of adaptively sampled ECG signals. This reduction in the data-rate not only reduces the power consumption of the ADC but also it significantly reduces the power consumption of the DSP platform while maintaining good performance.

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