NEGATIVE CAPACITANCE CIRCUIT WITH TUNEABLE GAIN MARGIN

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Abstract: A negative capacitance circuit with tuneable gain margin has been proposed. Gain margin of the proposed circuit is hardly affected by gain peaking of a gain stage. Thus, the proposed circuit is stable with a low gain margin. Also, the proposed circuit has higher input impedance and better closed-loop responses than those of a conventional circuit.

Introduction

Bioimpedance analysis is a promising area with many applications [1]. However, the input capacitance of a front-end for detecting a voltage results in loading errors, current leakages, and decreasing common-mode rejection ratio [2,3]. To cancel the input capacitance, a negative capacitance circuit has been used [4]. The circuit was also used to cancel the output capacitance of a current source [5,6]. This negative capacitance circuit applies positive feedback to the input terminal of a non-inverting gain stage from its output terminal through a capacitor. However, because loop gain of the circuit is limited by a dominant-pole of the gain stage, the loop gain has a maximum near the dominant-pole of the gain stage. Therefore, we found the following disadvantages of the conventional circuit: i) Selection and realization of the proper bandwidth of the gain stage is not easy. ii) Even though electrode impedance has been changed, gain margin is not easy to adjust. iii) Gain margin disappears and the circuit tends to oscillate if a gain peaking near the dominant-pole of the gain stage is created due to stray capacitances of the inverting input terminal of the non-inverting gain stage. In this presentation, a new circuit is proposed to remove the disadvantages.

Proposed Circuit, Circuit Analysis and Simulation

Figure 1. a) shows an equivalent circuit of the voltage measurement in bioimpedance analysis. At high frequency, a voltage follower is modelled as it is ideal except it has input capacitance C_{in} between the voltage follower and an electode. Electrode impedance which usually modelled as a resistor and a capacitor connected serially with each other is modeled as a resistor R_e, since impedance of the capacitor decreases at high frequency. The conventional negative capacitance circuit may be represented as in Fig. 1. b). It uses a capacitor for positive feedback and a band-limited gain stage for controlling loop gain. A wideband voltage follower is inserted to compare with the proposed circuit. Figure 1. c) shows the new negative capacitance circuit proposed in this presentation. The proposed circuit employs a wideband gain stage of gain A_o. In order to limit loop gain, a trimmer resistor R_f is connected serially to a feedback capacitor C_f. To measure input voltage, a wideband voltage follower is inserted to compare with the proposed circuit.

Analysis and simulation of the cicuits were carried out with: 1 kΩ of an electrode resistance R_e, 4 pF of the input capacitance C_{in}, 4 pF of the feedback capacitance

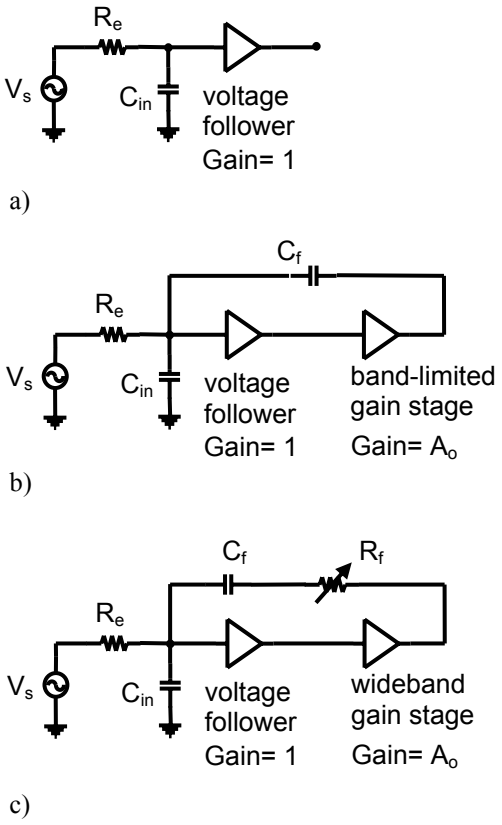

Figure 1: Equivalent circuit of voltage measurement in bioimpedance analysis using a) a voltage follower, b) a conventional negative capacitance circuit, and c) a proposed negative capacitance circuit

ISSN: 1727-1983

C_f, and 2 V/V of the gain stage's gain A_o. A conventional circuit, comprised a voltage follower and a gain stage, was compared with the proposed circuit. All amplifiers including the gain stage of the proposed circuit were modeled as ideal except that each voltage follower had an input capacitance and that the gain stage of the conventional circuit had a dominant-pole.

Fig. 2 shows loop gains of the conventional circuit and the proposed circuit when gain margins of the two circuits are identical as 6 dB. For the proposed circuit, the feedback resistor R_f controls maximum loop gain and the frequency at which the loop gain becomes a maximum. The maximum of loop gain of the proposed circuit is given by:

Maximum of loop gain
= 1/ gain margin
= $1/(1+R_f/A_oR_e)$

In practice, a gain peaking may occur. However, because the gain stage used in the proposed circuit is wideband, the frequency at which the gain peaking occurs is higher than the frequency of the maximum loop gain. Thus, the loop gain at the frequency of gain peaking is not so high that stability can be secured. Also, for the proposed circuit, phase-lead compensation to the gain-stage to remove the gain peaking can be done without changing its loop gain at a lower frequency range. Input impedance Z_{in} of the proposed circuit is given by:

$$Z_{in}= -(1+j\omega/((A_o-1)\omega_f))((A_o-1)\omega_f/\omega^2C_{in})$$

where $\omega_f=1/R_fC_{in}$

Thus, cancellation of the input capacitance is limited to a cancellation frequency of $(A_o-1)\omega_f$. This can be seen in Fig. 3 where input impedances of the proposed and conventional circuits, when the gain margin was set to 6 dB, were compared. In the Figure, the input impedance of a voltage follower without a negative capacitance circuit shown in Fig. 1. a) was also compared and is indicated as 'follower' in Fig. 3. The impedance is that of the input capacitance C_{in}. Fig. 3 shows that the impedance of the proposed circuit is 6 dB higher than that of the conventional one in a whole frequency range.

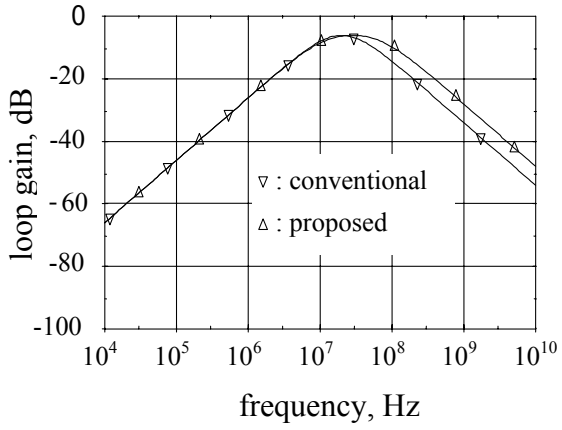

Figure 2: Loop gains of the conventional and proposed negative capacitance circuits

Closed-loop gains at the output terminals of the two voltage followers are shown in Fig. 4. For a gain margin of 6 dB, the voltage follower showed the highest frequency at which the closed-loop gain deviates from unit. The proposed circuit showed the next highest. The conventional circuit has the lowest one.

Fig. 5 shows closed-loop phase delays taken from the voltage followers of each circuit when the gain margin is 6 dB. The proposed circuit showed the highest frequency at which the phase delay occurs while the conventional circuit showed the next highest. The phase delay of the buffer at 1 MHz is unacceptably large. Even larger phase delay has been observed at output terminal of the gain stage of the conventional circuit. From the point that phase information is important for bioimpedance analyses, it is notable that the proposed circuit has the highest frequency for phase deviation.

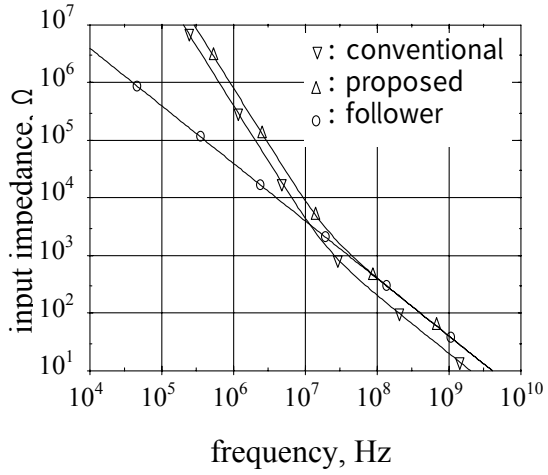

Figure 3. Input impedances of the conventional and proposed negative capacitance circuits

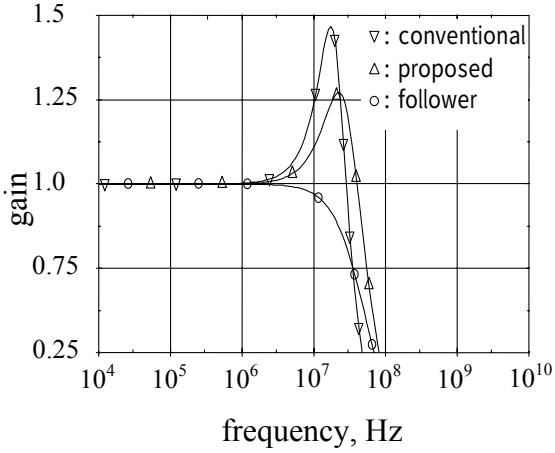

Figure 4: Closed-loop gains of the conventional and proposed negative capacitance circuits

ISSN: 1727-1983

Though the results presented above is only for a gain margin of 6 dB, it is obvious that lower gain margin results in higher input impedance and better closed-loop responses.

Experimental Results

A cascade of a voltage follower and a variable-gain gain stage was implemented using operational amplifiers of 300 MHz unit-gain frequency. Four-layer printed circuit board (PCB) was used and layout was done with caution to minimize stray capacitance. The gain stage was a non-inverting amplifier which comprised a negative feedback resistor of 470 Ω and a 1 kΩ trimmer resistor connected between inverting input terminal and ground. The input capacitance of the cascade, measured with a HP4192A impedance analyzer, without positive feedback, was measured as a constant value of 4.1 pF up to 4 MHz.

Gain peaking property of the cascade was observed and is shown in Fig. 6. In Fig. 6, Cc represents compensation capacitor connected in parallel to the 470 Ω negative feedback resistor. When any compensation capacitor is not used, gain peaking occured at 150 MHz. Gain peaking could be removed with a 4 pF compensation capacitor as shown in the Figure.

And then, a feedback capacitor C_f of 4 pF, a trimmer of 10 kΩ for the feedback resistor R_f, and a resistor of 1 kΩ for the electrode resistance R_e were added to complete the proposed negative capacitance circuit. By using the impedance analyzer, the input capacitance was cancelled at 100 kHz by controlling the gain of the gain stage. The output signal of the voltage follower was observed with a oscilloscope to check the stable operation. The proposed circuit showed stable operation and the input capacitance was measured as 0.0 pF up to 1 MHz. Because the proposed circuit is robust to a high frequency gain peaking, the feedback resistor R_f could be reduced to 500 Ω without oscillation.

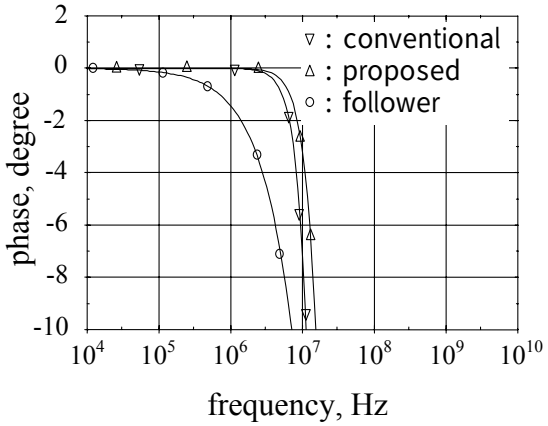

Figure 5: Closed-loop phase delay of the conventional and proposed negative capacitance circuits

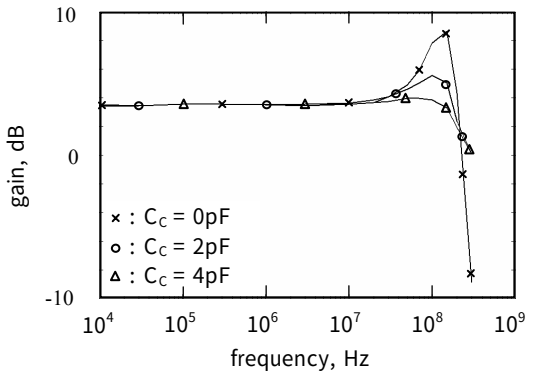

Figure 6: Gain peaking property of the implemented cascade

Furthermore, after reducing gain peaking with a shunting capacitor of 2 pF to the negative feedback resistor (470 Ω) of the gain stage, the circuit showed stable operation and cancellation of the input capacitance.

Figure 7 shows input impedance measured while changing the positive feedback trimmer R_f. At first, admittance was measured with the impedance analyzer and then the result was inverted to get impedance. Impedance variation with both frequency and feedback trimmer is consistent with the circuit analysis and simulation. As frequency increases, impedance decreases at a slope of -40 dB/dec. It is notable that the input capacitance is cancelled even with such a low gain margin of 1.1 (0.8 dB) set by trimming the feedback resistor R_f to 200 Ω. Therefore, it is confirmed experimentally that the proposed circuit operates stably even with a very low gain margin.

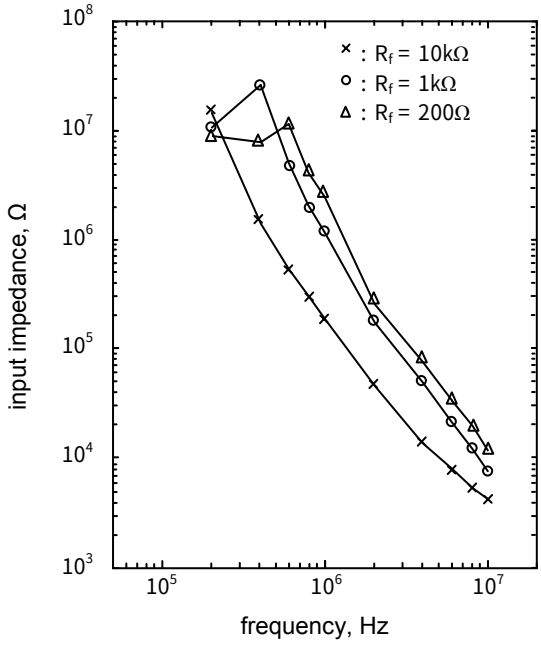

Figure 7: Measured impedance of the implemented circuit proposed in this presentation

ISSN: 1727-1983

Conclusion

A new negative capacitance circuit comprising wideband gain stage has been proposed. The proposed circuit is convenient in that its gain margin is tuneable with a feedback resistor R_f. The proposed circuit has higher input impedance and better closed-loop responses than those of a conventional circuit. It is confirmed experimentally that the proposed circuit operates stably even with a very low gain margin.

References

[1] BOONE, K. G., HOLDER, D. S.(1996): 'Current approaches to analogue instrumentation design in electrical impedance tomography', Physiol. Meas., **17**, pp. 229-247

[2] RIU, P. J., ROSELL, J., LOZANO, A., PALLAS-ARENY, R.(1995): 'Multi-frequency static imaging in electrical impedance tomography: Part 1 instrumentation requirements', Med. Biol. Eng. Comp., **33**, pp. 784-792

[3] JENNINGS, D., SCHNEIDER, I. D.(2001): 'Front-end architecture for a multi-frequency electrical impedance tomography system', Med. Biol. Eng. Comput., **39**, pp. 368-374

[4] RIGAUD, B., RECORD, P. M., ANAH, J., MORUCCI, J. P.(1991): 'Active electrodes for electrical impedance tomography: The limitation of active stray capacitance compensation', Ann. Int. Conf. of the IEEE Eng. in Med. and Biol. Soc., **13**, pp. 1587-1588

[5] GISSER, D. G., NEWELL, J. C., SAULNIER, G., HOCHGRAF, C., COOK, R. D., GOBLE, J. C.(1991): 'Analog electronics for a high-speed high precision electrical impedance tomography', Ann. Int. Conf. of the IEEE Eng. in Med. And Biol. Soc., **13**, pp. 24-25

[6] COOK, R. D., SAULNIER, G. J., GISSER, D. G., GOBLE, J. C., NEWELL, J. C., ISAACSON, D.(1994): 'ACT3: A high-speed, high-precision electrical impedance tomography', IEEE Trans. Biomed. Eng., **41**, pp. 713-72

ISSN: 1727-1983