ELECTROMAGNETIC COUPLINGS IN MICROSYSTEMS FOR MEDICAL APPLICATIONS

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Abstract: The main target of the paper was the solution of electromagnetic compatibility in integrated circuits (IC) and microsystems for medical applications. The electromagnetic compatibility serves as a measure for the possibility of co-existence of numerous electronic systems occupying a common environment without unwanted electromagnetic couplings that could interfere with correct functioning of individual systems. The microsystems, for example cardiac pacemaker, can be assumed to be independent electronic systems set up of individual operational blocks. The conveying of signals between blocks is provided by networks of electrical leads. Unwanted electromagnetic couplings do appear between leads inside the integrated circuit. During the process of signal propagation along the leads, parasitic electromagnetic couplings can cause interference in other signal leads. Such as interference can result in random disturbances in the microsystem. So, in solving the electromagnetic compatibility in microsystems, a considerable stress must be given to correct determination of parasitic electromagnetic couplings in the connecting lead systems.

Introduction

The electromagnetic compatibility (EMC) is one of the most important reliability parameters of electronic systems and devices. When EMC effects are properly taken care of during the design, the additional work and expense will return handsomely in a better reliability and competitiveness of the final product [1].

For optimum efficiency of microsystems composed of both discrete and integrated devices it is required that the changes of states of the active devices are performed as quickly as possible. The rapid variations of voltage and the resulting rapid variations of current create time-variable electric and magnetic fields around the devices and, even more important, around the connecting electric leads. These fields can cause operational faults in the device itself as well as in electronic systems located in close vicinity, sometimes even at larger distances.

Software tools kept emerging lately, permitting relatively detailed simulations of the effects connected to the propagation of time-variable signals along metallic lines. Unfortunately, in practical application these tools have proven to be rather inaccurate. Of course the accuracy of simulation procedures is limited when applied to real situations due to, among others, the degree of knowledge of the physical parameters of the simulated system.

Solution

In order to simplify the simulations of electronic systems and lead systems we have designed a method of forecasting the parasitic mutual couplings in a lead system using simple circuit models of connecting lines with crosstalks [2]. These models can be inserted in the electrical circuit connections of the systems to be simulated and so the crosstalk effects in well-defined digital systems can be analyzed. The same approach can be applied to on-chip interference inside integrated electronic devices.

A complete equivalent circuit of a twin-lead line close to a grounded plane is shown in Fig. 1. It was designed as a symmetrical PI-network including mutual magnetic coupling.

The parameters of the line equivalent circuit are: capacitances C_C (mutual lead-to-lead capacitance) and C_S (the lead-to-ground plane capacitance), inductances L_L (self-inductance of the lead), M (mutual inductance of the leads) R_L (lead resistance).

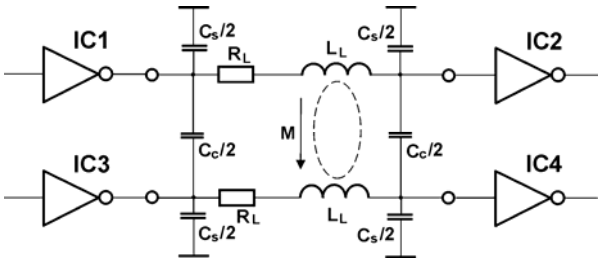

Figure 1: Complete equivalent circuit of a twin line with a grounded plane

Capacitive coupling is the dominant effect in high-impedance circuits like unipolar ICs in CMOS technology.

The influence of inductive coupling can be neglected in these circuits and thereby the equivalent circuit simplified to a circuit of twin leads with parasitic capacitive coupling only (see Fig. 2).

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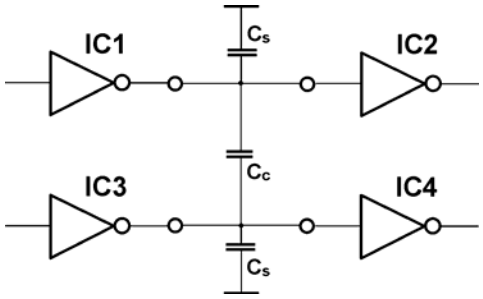

Figure 2: Simplified equivalent circuit of with a grounded plane

Figure 3 shows a twin lead line inside an integrated circuit in 2.4 μm Mietec CMOS technology. The lead dimensions correspond to the design rules for this technology.

Further there are indicated the leads parasitic capacitances: C_C – the mutual capacitance between the A and B a twin line leads, and C_S – the lead-substrate capacitance, all according to the simplified equivalent circuit (Fig. 2).

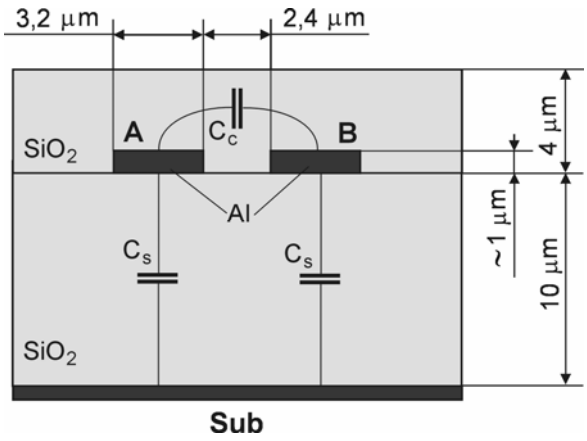

Figure 3: A twin line in a Mietec 2.4 μm CMOS IC; the leads are aluminum tracks inside the SiO_2

Simulation

The actual magnitude of crosstalk between leads inside an integrated circuit depends on the geometric parameters of the line and on the electrical parameters of gates connected to the line.

Most of the geometric parameters of the line are usually predetermined by the design rules of the particular technology. The electrical parameters of the gates are bound to the standard digital cell libraries and the designer can only select from a limited assortment of available digital cells.

In general, it can be expected that the crosstalk magnitude will rise with increasing length of mutually influencing leads. Results of parametric simulations for various line lengths are shown in Fig.5.

The graphs show the time-dependent voltage at the far end of the non-active line. A non-active line in an interference-free situation is assumed to be in the state of logical zero. The interfering impulses are transferred by parasitic capacitive coupling. The interference source was a CMOS gate-driven line, with the gate operating off a U_{CC} = 5V power supply, generating a rectangular waveform signal (Fig. 4).

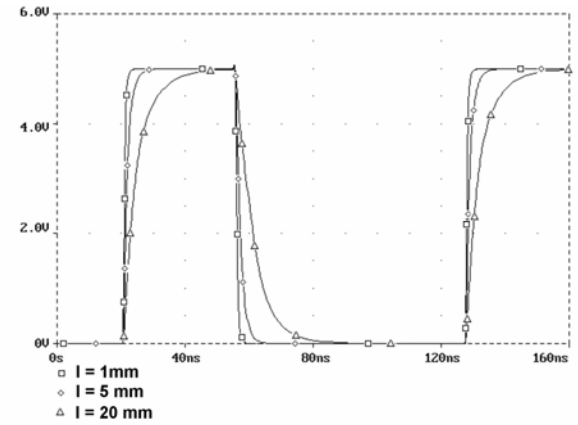

Figure 4: Waveforms at the far end of the active (interfering) line

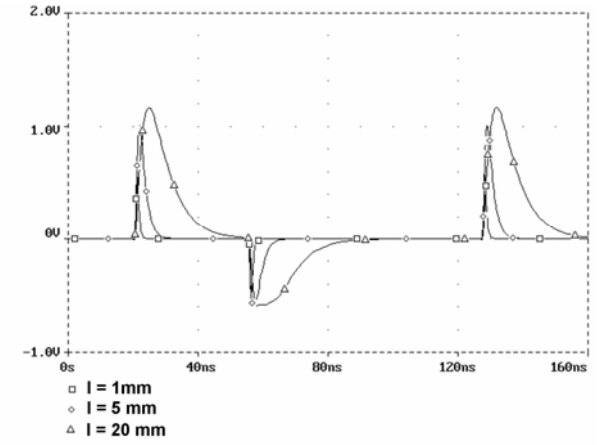

Figure 5: Waveforms at the far end of the non-active (interfered) line

Plotting the parametric simulation results in a graph showing the interfering pulse amplitude versus line length (Fig. 6), we can see that the crosstalks indeed rise with increasing line length but that the rate of rise drops. It can be stated that the amplitude of the interfering pulses is asymptotically approaching a certain maximum value.

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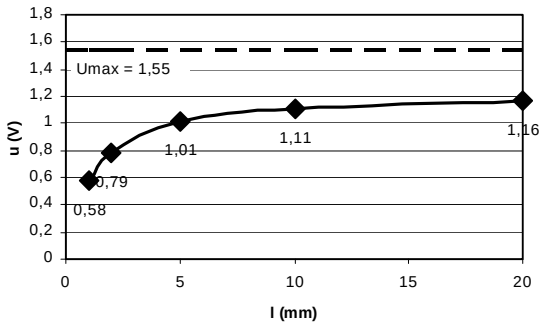

Figure 6: A plot of interfering impulse *u* versus line length *l*

The limit case

In order to be able to derive the maximum crosstalk amplitude regardless of the line length it is necessary to adjust the simplified IC twin-lead line equivalent circuit (Fig. 2) into a form permitting to set up the crosstalk transfer function. This equivalent circuit adjusted for AC crosstalk analysis (Fig. 7) contains capacitances C_V and C_S with the same meaning as in Figs. 2 and 3, the capacitance C_S must also include input capacitances of the gates connected to the line.

The driving CMOS gates connected to the line were transformed to resistors with a value *R*, representing the actual resistance of the MOS transistor in the "on" state.

The interference source is represented by the driving gate connected to the active line, in this case a U_Z voltage source while the interference receiver is a gate connected to the far end of the non-active line, in this case the interference is represented by the U_P voltage.

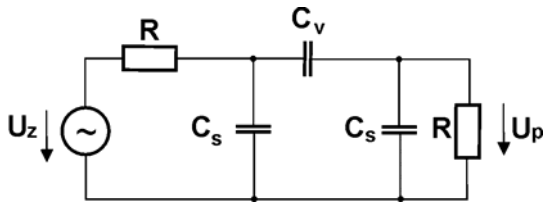

Figure 7: Adjusted equivalent circuit for A.C. analysis

The adjusted circuit (Fig. 7) was used to set up the crosstalk transfer function (1) in the form of a ratio of the U_P voltage at the interference receiver input to the U_Z voltage from the interference source. It is also possible to consider this transfer function to be a coupling coefficient showing the measure of coupling between the interference receiver and transmitter.

$$P = \frac{U_P}{U_Z} = \frac{j\omega RC_V}{-\omega^2 R^2 C_S(C_S + 2C_V) + 2j\omega R(C_S + C_V) + 1} \qquad (1)$$

Differentiating the transfer function *P* against the angular frequency ω we can find a local maximum and so find the critical frequency ω_0 for which the maximum transfer takes place. By setting the ω_0 frequency into the transfer function equation (1) we can find the maximum transfer P_0.

$$P_0 = \frac{1}{2}\frac{C_V}{C_V + C_S}, \qquad (2)$$

$$\omega_0 = \frac{1}{R\sqrt{C_S^2 + 2C_S C_V}} \qquad (3)$$

No resistances *R* appear in equation (2). From that follows that a long as the driving gates connected to the interfering and interfered lines have the same internal resistance, it will have no effect on the maximum coupling coefficient.

Timing errors

Another effect due to the parasitic couplings in electronic systems are timing errors. These effects are caused by mutual coupling between two active lines, i.e. both lines are transmitters and receivers of interference at the same time. Especially dangerous is mutual influencing of two lines carrying time-shifted similar signals.

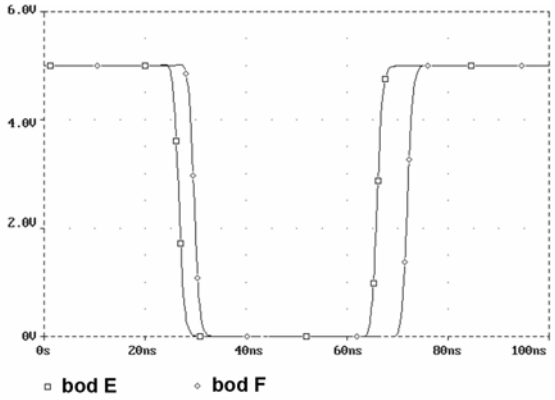

Figure 8: Voltage waveforms at the outputs of gates IC2 and IC4 connected two separate lines with parasitic coupling.

Fig. 8 and Fig. 9 show input voltage waveforms of gates IC2 and IC4 whose inputs are connected to the far ends of two lines (see Fig. 1). The gates IC1 and IC 3 are driven by digital signals with waveforms that are equal except a time shift of 3 ns. Fig. 8 shows the waveforms at the gate outputs (point E - output of the IC2 gate, point F - output of the IC4 gate) in the absence of parasitic coupling, and Fig. 9 with the parasitic capacitive coupling present.

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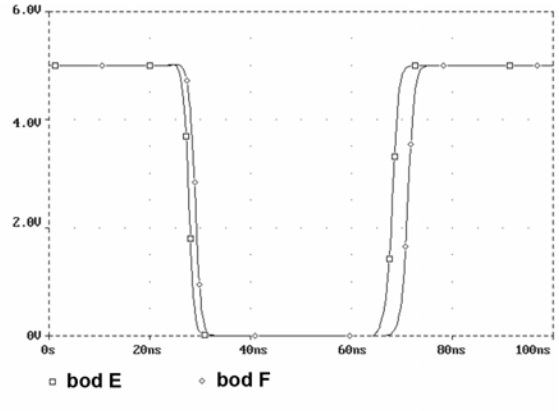

Figure 9: Voltage waveforms at the outputs of gates IC2 and IC4 connected to two lines with mutual parasitic capacitance.

By comparing the figure we can see that the mutual time shift between the signal was decreased by the effect of the coupling. This may result in errors, especially in synchronous digital systems requiring a certain advance of data at the input of a flip-flop or a register before the critical edge of the clock signal arrives at its input terminal. The parasitic capacitive coupling is just the effect that can cut this advance below permissible limits and cause an error in the system.

Conclusions

Applying the equation (2) to a particular twin-lead line in an IC, according to Fig. 3, it is possible to determine the maximum value of inter-line crosstalk. The numerical values of parasitic capacitances C_V and C_S were found with the aid of finite-element modeling of the electric field distribution [4].

Assuming the interfering voltage $U_Z = U_{CC}$ =5 V and applying the equation (2) we can find the maximum voltage at the interference receiver input as U_P = 1.55 V. The value of this UP voltage is, at the same time, equal to the maximum interfering pulse amplitude $U_{max} = U_P$ that can appear regardless of the line length.

The maximum value of the U_{max} impulse is shown in the graph (Fig. 6) as the theoretical maximum interference value which can never be exceeded even in the case of infinitely long lines.

By application of this method it is possible to forecast the maximum value of crosstalk between connecting lines inside a microsystem without the need to resort to time-consuming analog simulations respecting the parasitic coupling effects.

Acknowledgments

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